In the Specification:

On page 5, paragraph beginning at line 11, amend as follows:

If the read after write dependence is present, it is necessary to execute the instructions in the program sequences. It is, however, likely that an address of the load/store instruction has been unknown until the instruction is ~~bout~~about to be executed. Namely, it is likely that the dependence has been unknown until the execution of the instruction. For this reason, a disadvantage in performance of the processor by the inhibition to the non-program sequence execution is large.